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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/823,537	04/14/2004	Hsien-Yueh Hsu	4443-0111PUS1	4436

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EXAMINER	
TRAN, VINCENT HUY	

ART UNIT	PAPER NUMBER
2115	

NOTIFICATION DATE	DELIVERY MODE
06/13/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mailroom@bskb.com

Office Action Summary	Application No.	Applicant(s)	
	10/823,537	HSU, HSIEN-YUEH	
	Examiner	Art Unit	
	Vincent T. Tran	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 April 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is responsive to the communication filed on 4/30/07

2. Claims 1-13 are pending for examination.

3. The text of those sections of Title 35, U.S. code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claim 1, 7, 10 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. There is a different from the claimed "redeploy whole system resource shared by all the devices" with the "redeploy the system source shared by each device."

The specification specifically teaches the system source (partial or unused source) can be readjusted according the flow rate and not where in the specification does it teaches the redeployment of the whole system resource.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

8. Claim 10-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwazaki in view of Messick et al. US 20040044770 ("Messick").

9. As per claim 10, Iwazaki teaches a method for adjusting the system performance of a computer, for monitoring the actual data flow rates of devices fabricated on a motherboard and adjusting the operating rates of said devices, said method comprising the steps of:

(1) executing a program to make one selected said device be in an operating state [inherent];

(2) measuring a flow rate of data of said selected device in said operating state [col. 6 lines 53-59];

(3) defining a predetermined flow rate of said selected device according to said flow rate of data measured in said step (2) to indicate said selected device is in a busy state [NUM1, NUM2 - From col. 6 line 59 to col. 7 line 13];

repeating said steps (1).about.(3) to define the predetermined flow rates of said devices fabricated on said motherboard [col. 7 lines 9-13];

measuring actual data flow rates of said devices on said motherboard;

ascertaining operating state of all the devices;

comparing the operating states of all the devices and adjusting the operating rate of each device[fig. 3];

Although, Iwazaki specifically teaches a method for reducing electric power consumption of the processing apparatus by controlling the operating rates of the devices fabricated on a mother board in response to the load state of the bus; however, Iwazaki fails to teach the redeploying whole system resource shared by all the devices.

Messick teaches another invention directed to a method of managing system resource allocation in a apparatus that receiving a plurality of I/O requests from a plurality of devices wherein each devices is connected to the apparatus via a separate port. Specifically, Messick teaches monitoring the activity at each port [paragraph 0030-0031], comparing the operating state of all the devices [paragraph 0030-0031 – if activity a specific port drop below a threshold], and redeploy whole system resource shared by all the devices [paragraph 0035-0036].

At the time of the invention was made, it would have been obvious to one of ordinary skill in the art to have modified the system of Iwazaki with the redeploy whole system resource shared by all the devices in response to the load state at each port of Messick.

The advantages is that it allow the apparatus to operate in a more efficient manner by dynamically optimizes the system resource.

10. As per claim 11, Iwazaki teaches said flow rate of data is the number of times of accessing data passing through said device per unit time [2C, 2E fig. 2].

11. As per claim 12, Iwazaki teaches said flow rate of data is the number of times of transferring commands through said device per unit time [2D fig. 2].

12. As per claim 13, Iwazaki inherently teaches devices connected to said performance control chip comprise a CPU [2 fig. 5], a north bridge chip, a south bridge chip, an AGP slot, PCI slots and a motherboard power supply.

13. Claims 1-2, 4, 6-8, 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Filippo U.S. Patent No. 6,976,182 in view of Jacobson U.S. Patent 6,915,518 or Messick.

14. As per claim 1, Filippo teaches an apparatus for adjusting the system performance of a computer, fabricated on a motherboard, said apparatus comprising:

a plurality of performance monitor means [102a fig. 1], connected respectively to bus lines [106b, b fig. 1] which are connect with devices [104a, b fig. 1] mounted on the motherboard, for monitoring the operating state of each device according to the flow rate of data transferred in the bus line[col. 7 lines 4-9]; and

a performance control chip [102 + 204 fig. 1-3], connected separately to the devices, for adjusting the operating rate of the devices responsive the performance monitor means, the performance control chip being capable of ascertaining the operating state of each the device is busy or not by comparing the operating state of each device[col. 7 lines 44-61].

Filippo teaches the performance control chip being capable of ascertaining the operating of each device is busy or not so as to supply power the device. However, Filippo does not teach redeploy whole system resource shared by all the devices.

Jacobson teaches another system and method directed to the runtime reallocation of resources in response to changing activity level. Specifically, Jacobson teaches a load monitor is coupled to the PLDs for monitoring the activity level of the functions wherein, if the traffic on the channels implemented a first protocol has decrease and the traffic on the channels implementing a second protocol has increases, the load monitor redeploy the PLD resources shared by all function [col. 2 lines 21-32, 46-59; col. 3 line 52 to col. 4 line 11].

Messick teaches another similar method for dynamically reallocating bandwidth resource in response the activity measure at each port [see discussion above].

Therefore, at the time of the invention was made, it would have been obvious to one of ordinary skill in the art to have combine the teaching of Jacobson or Messick discussed above with Filippo in order to improve the system performance by provide the system the ability to dynamically optimizing the whole resource shared by all the device during the runtime of the system in response the changing in activity level of each device.

15. As per claim 2, Filippo only teaches the activity detector may be performed by monitoring control signals or by monitoring the flow of data across the bus of each functional unit. Filippo does not explicitly teach the bus lines comprises a PCI bus line, connected between a south bridge chip and a PCI slot; an AGP bus line, connected between a north bridge chip and an AGP slot; a RAM bus line, connected between said north bridge chip and a RAM device; and a CPU bus line, connected between a CPU and said north bridge chip. However, it is obvious to one of ordinary skill in the art that the generic bus line of Filippo encompasses the

specific well know claimed bus lines since the special bus lines do not alter the performance of Filippo system.

16. As per claim 4, Filippo inherently teaches performance monitor means comprises a counter, for measuring the number of times of transferring commands or accessing data through one selected said bus line per unit time [col. 7 lines 4-9].

17. As per claim 6, Filippo teaches the performance control chip is connected to a power supply and is capable of controlling the operating rate of the device by adjusting the power supplied thereto [fig. 3].

18. As per claim 7, Filippo teaches an apparatus for adjusting the system performance of a computer, fabricated on a motherboard, said apparatus comprising:

a counters [inherent], coupled respectively to the corresponding one of bus lines [106a fig. 1] which are connected with devices, for measuring the flow rate of data transferred in each said bus line per unit time [col. 7 lines 4-9]; and

a performance control chip, connected separately to said devices, being capable of ascertaining each said device is busy or not [see discussion in claim 1];

said performance control chip comprising

a register [inherent], for storing predetermined flow rates of said devices;

a comparator [inherent], for comparing actual flow rates measured by said counter with said predetermined flow rate stored in said register, when said actual flow rate of one said device exceeds said predetermined flow rate thereof, said device is ascertained to be busy [abs].

and Jacobson or Messick teaches redeploying whole system resource share by all the device in response the activity level [see discussion in claim 1].

19. As per claim 8, see discussion in claim 2.

20. As per claim 10, the claim is substantially the same as of claim 1 and 7; therefore, it is rejected for the same reason discussed above.

21. As per claim 11, Filippo teaches said flow rate of data is the number of times of accessing data passing through said device per unit time [col. 7 lines 4-9].

22. As per claim 12, Filippo teaches said flow rate of data is the number of times of transferring commands through said device per unit time [col. 7 lines 4-9].

23. Claims 1-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gunther et al. U.S. Patent No. 5,781,783 ("Gunther") in view of Jacobson or Messick

24. As per claim 1, Gunther teaches an apparatus for adjusting the system performance of a computer, fabricated on a motherboard, said apparatus comprising:

a plurality of performance monitor means [60 fig. 3, 84 fig. 3], connected respectively to bus lines [12 fig. 1; 85 fig. 4] which are connect with devices [32 fig. 3, 82 fig. 4] mounted on

the motherboard, for monitoring the operating state of each device according to the flow rate of data transferred in the bus line[94 fig. 5; 84 fig 4]; and

a performance control chip [60 fig. 3], connected separately to the devices, for adjusting the operating rate of the devices responsive the performance monitor means, the performance control chip being capable of ascertaining the operating state of each the device is busy or not by comparing the operating state of each device[fig. 5].

Gunther teaches the performance control chip being capable of ascertaining the operating of each device is busy or not so as to provide clock to the device. However, Gunther does not teach redeploy whole system resource shared by all the devices.

Jacobson teaches another system and method directed to the runtime reallocation of resources in response to changing activity level. Specifically, Jacobson teaches a load monitor is coupled to the PLDs for monitoring the activity level of the functions wherein, if the traffic on the channels implemented a first protocol has decrease and the traffic on the channels implementing a second protocol has increases, the load monitor redeploy the PLD resources shared by all function [col. 2 lines 21-32, 46-59; col. 3 line 52 to col. 4 line 11].

Messick teaches another similar method for dynamically reallocating bandwidth resource in response the activity measure at each port [see discussion above].

Therefore, at the time of the invention was made, it would have been obvious to one of ordinary skill in the art to have combine the teaching of Jacobson or Messick discussed above with Gunther in order to improve the system performance by provide the system the ability to dynamically optimizing the whole resource shared by all the device during the runtime of the system in response the changing in activity level of each device.

25. As per claim 2, Gunther teaches bus lines comprises a CPU bus line [12 fig. 1], connected between a CPU and the north bridge chip [inherent].

26. As per claim 3, Gunther teaches the devices connected to the performance control chip comprises a CPU [14 fig. 1].

27. As per claim 4, Gunther teaches the performance monitor means comprises a counter [64 fig. 3], for measuring the number of times of transferring command or accessing data through one selected the bus line per unit time.

28. As per claim 5, Gunther teaches a register [68 fig. 3], for storing predetermined flow rates of said devices; a comparator [66 fig. 3], for comparing actual flow rates provided by said performance monitor means with said predetermined flow rates stored in said register, when said actual flow rate of one selected said device exceeds said predetermined flow rate thereof, said device is ascertained to be busy.

29. As per claim 6, Gunther teaches the performance chip is connected to a mother board power supply on the motherboard and is capable of controlling the operating rate of each the device by adjusting the power supplied thereto [col. 11 lines 1-8].

30. As per claim 7, Gunther teaches an apparatus for adjusting the system performance of a computer, fabricated on a motherboard, said apparatus comprising:

a plurality of counters [64 fig. 3 and not show in 84 fig. 4], coupled respectively to the corresponding one of bus lines [12 fig. 1 or 85 fig. 4] which are connected with devices [32 fig. 3 or 82 fig. 4], for measuring the flow rate of data transferred in each said bus line per unit time [fig. 5, 6 and 7]; and

a performance control chip, connected separately to said devices, being capable of ascertaining each said device is busy or not [60 fig. 3];

said performance control chip comprising

a register [68 fig. 3], for storing predetermined flow rates of said devices;

a comparator [66 fig. 3], for comparing actual flow rates measured by said counter with said predetermined flow rate stored in said register, when said actual flow rate of one said device exceeds said predetermined flow rate thereof, said device is ascertained to be busy [fig. 5, 6].

and Jacobson or Messick teaches redeploying whole system resource share by all the device in response the activity level [see discussion in claim 1].

31. As per claim 8 and 9, see discussion in claim 2 and 3.

32. As per claim 10, Gunther teaches a method for adjusting the system performance of a computer, for monitoring the actual data flow rates of devices fabricated on a motherboard and adjusting the operating rates of said devices, said method comprising the steps of:

(1) executing a program to make one selected said device be in an operating state [inherent];

(2) measuring a flow rate of data of said selected device in said operating state [94 fig. 5; 114 fig. 6];

(3) defining a predetermined flow rate of said selected device according to said flow rate of data measured in said step (2) to indicate said selected device is in a busy state [106 fig. 5; 122 fig. 6];

repeating said steps (1).about.(3) to define the predetermined flow rates of said devices fabricated on said motherboard [loop in fig. 5 and 6];

ascertaining operating state of all the devices [64 fig. 3];

comparing the operating states of all said devices [66 fig. 3];

and Jacobson or Messick teaches redeploying whole system resource share by all the device in response the activity level [see discussion in claim 1].

33. As per claim 11, Gunther teaches said flow rate of data is the number of times of accessing data passing through said device per unit time [fig. 7].

34. As per claim 12, Gunther teaches said flow rate of data is the number of times of transferring commands through said device per unit time [fig. 7].

35. As per claim 13, Gunther inherently teaches devices connected to said performance control chip comprise a CPU [fig. 1], a north bridge chip, a south bridge chip, an AGP slot, PCI slots and a motherboard power supply.

Conclusion

36. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Examiner's note:

Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in entirety as potentially

teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

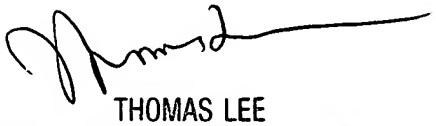
Prior Art not relied upon:

Please refer to the references listed in attached PTO-892, which, are not relied upon for claim rejection since these references are relevant to the claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent T. Tran whose telephone number is (571) 272-7210. The examiner can normally be reached on 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas c. Lee can be reached on (57 1)272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



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